



#4/B 815
6-27-02
M. Walsh

PATENT
Customer No. 22,852
Attorney Docket No. 4329.2270-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Shinsuke SAKAMOTO et al.

Application No.: 10/081,109

Filed: February 25, 2002

For: SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE AND WIRING
ARRANGING METHOD THEREOF

Commissioner for Patents
Washington, DC 20231

Sir:

SECOND PRELIMINARY AMENDMENT

Prior to the examination of the above application, please amend this application as follows:

IN THE CLAIMS:

Please amend claims 1 and 9-14, as follows:

1. (Twice Amended)

A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring layer in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged on a wiring layer different from said first I/O slot;

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